

Jan Arild Tofte

tofte@computer.org – <http://tofte.org>

Work Experience

- 7/00–present: Design–for–test Field Application Engineer at Mentor Graphics, San Jose sales office, California. As a technical member of the sales team, my job effort includes the following:
- Work with the sales team to identify and technically qualify new business opportunities.
 - Drive adoption of new technology and tool usage within the existing customer base.
 - Act as a trusted advisor and perform hands–on design work in a customer specific environment to prove tool capabilities during the benchmarking and evaluation process, as well as ensuring successful adoption after the sale.
 - Work closely with R&D and marketing to define and drive the continued improvement and future development of products.
 - Deliver and present workshops, lunch–and–learns, and product demonstrations to increase awareness and knowledge of tools and new technology trends within the technical community.
 - Communicate and present with impact to a wide customer audience at different levels of management.

As a DFT Field Application Engineer, my area of expertise includes the complete VLSI design–for–test flow: test synthesis, automatic test pattern generation (ATPG), memory testing, boundary scan (JTAG), logic built–in–self–test (LBIST), and embedded deterministic test (EDT), and logic simulation.

- 4/99 – 6/00: Design–for–test Corporate Application Engineer at Mentor Graphics, headquarter in Wilsonville, Oregon. I provided post–sales support for users of Mentor DFT products throughout North America. DFT tools covered: DFTAdvisor, FastScan, FlexTest, BSDArchitect, LBISTArchitect, and MBISTArchitect.
- 2/95 – 10/97 Part time job (full time during the 3 summers) at the [Molecular Beam Epitaxy \(MBE\) Lab](#) at UCSB. The research included the development of a multi–channel optical–based flux monitor for in–situ monitoring of MBE.

Education

- 3/97 – 3/99: Master of Science, electrical and computer engineering, University of California at Santa Barbara. Coursework depth in VLSI design and fabrication, and computer architecture. During my last year, I worked with Prof. Kwang-Ting (Tim) Cheng as a research assistant in the [VLSI Testing, Verification and Synthesis Group](#). The focus of my research was DFT for analog and mixed-signal circuits.
- 9/94 – 3/97: Bachelor of Science, electrical and computer engineering, University of California at Santa Barbara.
- 8/92 – 6/94: California State University, Fresno.
Major: electrical and computer engineering.
- 8/91 – 6/92: University of Bergen, Norway.
Major: Undeclared – math/science.
- 8/87 – 6/91: Four-year electronics technician degree earned at Bergen Technical College, Norway.

Technical Sales Skills

- Target Account Selling.
- Value Selling.
- Trusted advisor and technical presentation skills.
- Karrass effective negotiation skills.

Academic Teaching Experience

- Spring 98' and Fall 98': Teaching assistant for the ECE 255 graduate class in VLSI testing at UCSB. I was also a project mentor for students who used Mentor Graphics' DFT tools in their final project.
- Winter 99: Teaching assistant and lab instructor for ECE 152B – Digital Design Methodologies and Microcomputer–Based Design at UCSB.

Additional Skills

- Operating systems: Unix, Linux, Windows NT/98/2000/XP
- Computer Languages: Perl, C, Pascal, Fortran, LabVIEW.
- Foreign Languages: Scandinavian (Norwegian, Swedish, Danish), some German.
- Coursework and interest in international politics, international relations theory, and global political economy.

Published Work

- Xinli Gu, Jan A. Tofte, Sung Soo Chung, Frank Tsang, Hamid Rahmanian "[An effort-minimized logic BIST implementation method](#)," *Proceedings of IEEE International Test Conference, Baltimore, MA*, pp.1002–1010, October 2001.
- Xinli Gu, Jan A. Tofte, Sung Soo Chung, Frank Tsang, Hamid Rahmanian "[A Fast Timing Closure Technique for Industrial use of Logic BIST](#)," *IEEE European Test Workshop, Stockholm, Sweden*, May 2001.
- Jan Arild Tofte, Chee-Kian Ong, Jiun-Lang Huang, and Kwang-Ting (Tim) Cheng "[Characterization of a Pseudo-Random Testing Technique for Analog and Mixed-Signal Built-In-Self-Test](#)," *Proceedings of IEEE VLSI Test Symposium, Montreal, Canada*, pp. 237–246, May 2000.
- Paul Pinsukanjana, Andrew Jackson, Jan Tofte, Kevin Maranowski, Scott Campbell, John English, Scott Chalmers, and Arthur Gossard "[Real-time simultaneous optical-based flux monitoring of Al, Ga, and In using atomic absorption for molecular beam epitaxy](#)," *Journal of American Vacuum Society*, Vol. 14, No. 3, May/June 1996.
- Presentation at the 1995 Southern California conference on undergraduate research: Real time simultaneous optical-based flux monitoring of molecular beam fluxes during epitaxial growth.

Co-Authored Patents

- [U.S. Patent 6,075,558](#): "Integrated multi-channel optical-based flux monitor and method", June 13, 2000.
- [U.S. Patent 6,038,017](#): "Method of controlling multi-species epitaxial deposition.", March 14, 2000.
- [U.S. Patent 5,936,716](#): "Method of controlling multi-species epitaxial deposition.", August 10, 1999.

Personal

- Citizenship: Norwegian.
- U.S. Work Permit: Green Card.
- References: Available upon request.